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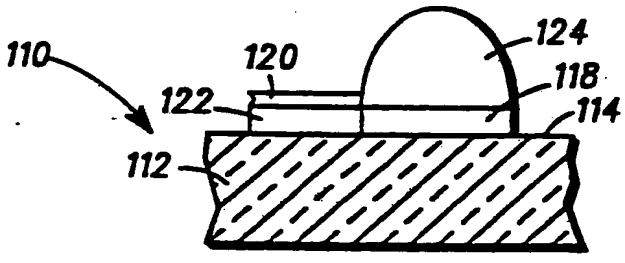

(57) Abstract

A solder bump (30, 124) is formed on a circuit trace by a method that includes depositing onto the trace a uniform thin plate (26, 124) of solder alloy and reflowing the solder alloy to form the bump. In one aspect of this invention, the trace comprises first and second linear sections (18, 20) that intersect at an intersection (22) whereat the bump is formed. In another aspect of this invention, the trace includes a terminal (116) having an enlarged terminal pad (118) connected to a runner section (120), whereupon the bump forms at the pad. The solder plate is deposited, preferably by electroplating, at a thickness between about 10 and 25 microns. Thereafter, when the trace is heated to melt the solder layer, the solder coalesces to form the bump having a height preferably greater than 40 microns.

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SOLDER PLATE REFLOW METHOD FOR FORMING A SOLDER BUMP ON A CIRCUIT TRACE

Background of the Invention

This invention relates to a method for forming a solder-bumped circuit trace on a printed circuit board or the like. More particularly, this invention relates to such method comprising reflow of a thin solder plate deposited on a circuit trace to cause the solder to coalesce to form a solder bump.

In the manufacture of a microelectronic package, it is known to mount an integrated circuit component onto a printed circuit board by solder bump interconnections. For this purpose, the board includes a copper circuit trace disposed on a dielectric substrate. To mount the component, a solder bump is attached to a bond pad on the component, typically by placing a preformed microsphere of the solder alloy on the pad and heating to reflow the solder. The bumped component is assembled with the board such that the bump rests against the trace at a predetermined site. The assembly is heated to reflow the solder so that, upon cooling to resolidify the solder, the solder is bonded to the trace as well as the component pad to physically join the component to the board and also to electrically connect the component to the trace for conducting electrical signals to and from the component for processing.

In the formation of solder bump interconnections, it has been proposed to apply a solder bump to the trace at the attachment site to provide additional solder in forming the interconnection. Also, as is known, it is convenient to apply the solder to a printed circuit board by electroplating. However, electroplating produces a generally uniform plate, in contrast to

a solder bump that provides an enlarged mass at the site. Thus, there remains a need for an improved method for preforming a solder bump on a circuit trace at a designated site.

Summary of the Invention

This invention contemplates a method for forming a solder-bumped circuit trace that includes depositing onto the trace a thin plate of solder alloy and reflowing the solder alloy to form a bump.

In one aspect of this invention, the trace comprises a first linear section and a second linear section that is disposed to intersect the first section at an intersection such that the angle between the sections is between 45 degrees and 135 degrees. The first trace section has a generally uniform width, typically less than 500 microns and preferably between 50 and 150 microns. The second trace section has a generally uniform width, which may be either equal to or different from the first section width, that also is typically less than 500 microns and preferably between 50 and 150 microns.

In another aspect of this invention, a solder bump is formed on a terminal that is configured to include an enlarged pad connected to a linear runner section that has a predetermined width. The width of the runner is suitably less than 500 microns and preferably between 50 and 150 microns. The enlarged pad has a width, measured parallel to the runner width, that is greater than the runner width.

In either event, the trace is formed of a solder-wettable metal, most commonly copper. Prior to reflow, the trace includes a thin, outer plate composed of the solder alloy and

having a uniform thickness. Thereafter, when the trace is heated to melt the solder layer, it is surprisingly found that the solder alloy coalesces either at the intersection or at the enlarged pad, to form the desired bump. In a preferred embodiment, the solder layer is deposited by electroplating to a thickness between about 10 and 25 microns and is reflowed to form a bump having a height greater than 40 microns and preferably between 60 and 80 microns.

In another aspect of this invention, a method is provided for manufacturing a printed circuit board that includes applying a copper plate onto a dielectric substrate and thereafter applying a photolithographic mask or the like onto the plate. The mask defines an opening that exposes the copper at the trace, but covers the copper plate on the region adjacent to the trace. The masked copper plate is immersed in an electroplating bath containing dissolved tin and lead ions and cathodically biased to codeposit tin and lead metal onto the exposed copper to form a thin solder plate. Thereafter, the mask is removed, and the plate is immersed in a copper etching solution. The solder coating protects the underlying trace copper, while the solution etches the exposed copper to define the trace. The trace is then heated to reflow the solder to form the bump.

Thus, this invention provides a convenient method for forming a solder bump on a circuit trace. The bump is formed from a thin solder plate, thereby reducing the plating time. The solder plate also advantageously serves as an etch mask prior to reflow, allowing the circuit trace to be defined and the solder deposited using but a single photolithographic mask. Even though the solder is deposited as a thin plate, when the trace is subsequently heated to melt the solder alloy, the solder nevertheless coalesces to form a bump of a sufficient mass for

use, for example, in attaching a component by solder bump interconnection.

Description of the Drawings

The present invention will be further illustrated with reference to the accompanying drawings wherein:

FIG. 1 is a partial plan view of a printed circuit board showing a circuit trace adapted for forming a solder bump in accordance with this invention.

FIG. 2 is a cross-sectional view of the printed circuit board in FIG. 1, taken along line 2-2, showing a solder-plated trace prior to reflow.

FIG. 3 is a cross-sectional view of the circuit trace in FIG. 2 following reflow of the solder plate to form a bump.

FIG. 4 is a partial plan view of a printed circuit board showing an alternate embodiment of a circuit trace for forming a solder bump in accordance with this invention.

FIG. 5 is a partial plan view of a printed circuit board showing still another embodiment of a circuit trace for forming a solder bump in accordance with this invention.

FIG. 6 is a partial plan view of a printed circuit board showing still another embodiment of a circuit trace for forming a solder bump in accordance with this invention.

FIG. 7 is a plan view of a printed circuit board showing terminals for forming solder bumps thereon in accordance with this invention.

FIG. 8 is a cross-sectional view of the printed circuit board in FIG. 1, taken along line 2-2, showing a terminal prior to solder reflow;

FIG. 9 is a cross-sectional view of the terminal in FIG. 2 following reflow of the solder alloy to form a bump.

FIG. 10 is an electron photomicrograph showing a solder bump formed on a printed circuit board in accordance with this invention.

FIG. 11 is a perspective view of a terminal on a printed circuit board having an alternate configuration suitable for forming a solder bump in accordance with this invention; and

FIG. 12 is a perspective view of a terminal on a printed circuit board showing still another configuration suitable for forming a solder bump in accordance with this invention.

Detailed Description of the Invention

In a first preferred embodiment, referring to FIGS. 1-3, the method of this invention is employed to form a printed circuit board 10 having a solder-bump circuit trace 12. Printed circuit board 10 comprises a dielectric substrate 14 of the type referred to as an FR4 card and composed of an epoxy resin and glass fiber laminate. Substrate 14 has a planar major surface 16 to which is affixed circuit trace 12. For purposes of illustrating the features of this invention, board 10 is only partially depicted in the figures, it being understood that the depicted region constitutes but a minor proportion of the total area and that circuit trace 12 extends onto other regions of the board for conducting electrical signals for processing. In

accordance with this invention, circuit trace 12 comprises a first linear section 18 and a second linear section 20, each having generally uniform width of about 100 microns. Sections 18 and 20 are arranged on surface 16 to intersect at an intersection designated generally at 22 and such that the angle between the sections is a right angle, i.e., 90 degrees.

Referring to FIG. 2, in accordance with the method of this invention, circuit trace 12 is initially formed of two coextensive metal layers 24 and 26. Layer 24 lies immediately adjacent substrate surface 16 and is formed of metallic copper having high electrical conductivity conducive to conducting electrical signals. Copper layer 24 is coated by a thin layer 26 composed of electroplated tin-lead solder alloy.

Printed circuit board 10 is manufactured by patterning a copper plate to define trace 12, including intersection sections 18 and 20, and electroplating solder onto the trace. Accordingly, a copper plate is initially applied to dielectric substrate 14 to completely cover surface 16. Thus, the plate includes a region for forming layer 24 of trace 12 and an adjacent region about trace 12. A suitable copper-plated board is readily commercially available and features a copper plate having thickness of about 17 microns. A film of photoimageable polymer material is applied to the copper plate and selectively irradiated to develop the polymer to form a photoresist mask. The mask is about 25 microns thick and covers the copper plate region about the trace and defines an opening whereat the trace layer 24 is exposed.

The masked board is immersed in a tin-lead plating solution and cathodically biased to deposit solder alloy onto the exposed copper trace. A suitable plating bath comprises, in water, 56.3 grams per liter tin, added as concentrated stannous

fluoborate solution; 26.3 grams per liter lead, added as concentrated lead fluoborate solution, 99.8 grams per liter fluoboric acid; 26.3 grams per liter boric acid and 19.5 grams per liter liquid peptone. The masked board is immersed in the bath at ambient temperature spaced apart from a tin-lead counterelectrode. An electrical potential is applied to the copper plate to negatively bias the copper relative to the counterelectrode and codeposit metallic tin and metallic lead onto the exposed copper surface. One advantage of plating the tin-lead deposited onto the copper plate prior to removing the unwanted copper about the trace is that the continuous plate facilitates distribution of the plating current to produce a uniform electrodeposit. The resulting plate is composed of about 40 percent lead and the balance tin and has a thickness of about 20 microns. The plate thickness is preferably less than the thickness of the mask, so that plating is confined to the opening above the trace and does not extend upon the mask surface.

Following plating, the board is immersed in an alkaline solution to strip the photoresist mask, thereby exposing the copper plate region about the solder-coated trace. The board is immersed in an aqueous copper-etching solution containing ammonium persulfate, following by a water rinse. The etching solution removes the exposed copper. However, the tin-lead alloy is resistant to attack by the etching solution and acts as a mask to protect the underlying copper trace. In this manner, the unwanted copper is removed from about the trace to complete fabrication of the solder-plated trace depicted in FIG. 2 and featuring the copper plate 24 coated with the uniform, thin solder plate 26.

The printed circuit board having the dual-layer trace 12 is heated to reflow the solder to form the desired bump on

intersection 22. A flux composed of amine hydrochloride and amine hydrobromide in isopropyl alcohol vehicle is applied to the solder plate surface. The board is immersed in hot polyoxyalkylene glycol bath at 250°C for 15 seconds. It was found that during immersion, the solder alloy melted and reflowed to draw solder from the sections onto intersection 22, thereby forming a bump 30 shown in FIG. 3. Following reflow, a residual solder film 32 remains on sections 18 and 20, but the thickness is significantly reduced compared to the initial film. Bump 30 has a height greater than 40 microns and preferably between 60 and 80 microns. Thus, bump 30 is particularly well suited for use in forming a solder bump interconnection to attach an electrical component to printed circuit board 10.

In the embodiment depicted in FIG. 1, sections 18 and 20 extend an indefinite length from intersection 22. This arrangement is particularly advantageous for allowing electrical signals to be conducted from a component attached to intersection 22, using bump 30, to or from distinct portions of the electrical circuit. However, the method of this invention is not limited to traces wherein both linear sections are active leads for the electrical circuit, but may be employed to produce a solder bump at an intersection wherein only one section is connected to the circuit.

Referring to FIG. 4, a printed circuit board 50 comprises a circuit trace 52 having an alternate configuration suitable for forming a solder bump thereon in accordance with the method of this invention. Trace 52 is disposed on a planar dielectric substrate 54 similar to substrate 14 in FIG. 1. Trace 52 comprises a first linear section 56 and a second linear section 58 that intersect at a right angle a' to form an intersection indicated generally at 60. In this embodiment, linear section

56 extends beyond the region depicted in FIG. 4 for connection to remote electrical features on board 50 to provide an active lead for conveying electrical signals to and from intersection 60. However, second section 58 is shortened and, except through the connection through lead 56, is not otherwise connected to the electrical circuit. As depicted in FIG. 4, trace 52 comprises a copper layer immediately overlying substrate 54 and a thin, uniform tin-lead solder electroplate. That is, trace 52 is shown following patterning of the copper layer and electrodeposition of the thin solder plate in a condition similar to FIG. 2, but prior to reflow of the solder alloy. Thereafter, trace 52 is heated, for example, by immersion in a hot oil bath, to melt the outer solder plate, whereupon the molten solder is drawn onto intersection 60 from the adjacent sections to form a solder bump.

The size of the bump formed during reflow is believed to be principally determined by the surface tension of the molten alloy and is independent of the length of the adjacent sections, provided that sufficient molten alloy is available for forming the bump. Thus, for linear sections of comparable widths, the size of the bump formed at intersection 60 of trace 52 in FIG. 4 is believed to be equal to the bump formed at intersection 22 of trace 12 in FIG. 1, with additional molten metal being drawn as needed from section 56 to compensate for any deficiency in the volume of metal drawn from section 58.

Referring to FIG. 5, in still another embodiment of this invention, a printed circuit board 70 includes a Y-shaped trace 72 suitable for forming a bumped intersection in accordance with this invention. Trace 72 is affixed to a dielectric substrate 74 and includes a first section 76 that extends for a remote connection to other electrical features on board 70 so as to act

as an active lead for the electrical circuit. Trace 72 further comprises shortened sections 78 and 80 that intersect trace section 76 at an intersection 82. Sections 76, 78 and 80 are disposed equiangularly about intersection 82 such that each angle a" between adjacent sections is 120 degrees. Trace 72 is shown prior to reflow and comprises an underlying copper layer immediately adjacent substrate 74 and a uniform, thin electroplate of tin-lead solder alloy, similar to trace 12 in FIG. 2. Thereafter, the trace is heated to melt the outer solder plate, whereupon the solder coalesces at intersection 82 to form a solder bump. In this embodiment, the two shortened sections 78 and 80 increase the volume of solder adjacent intersection 82 to be drawn by capillary action for forming the bump.

FIG. 6 shows yet another embodiment of a trace configuration suitable for forming a solder bump in accordance with this invention. A printed circuit board 90 comprises a dielectric substrate 92 having affixed thereto a trace 94. Trace 94 comprises a first linear section 96 that extends for connection to remote features of the electrical circuit to serve as an active lead. In addition, trace 94 includes three shortened linear sections 98, 100 and 102 that intersect section 96 and each other at an intersection designated generally at 104. The sections 96, 98, 100, and 102 are disposed equiangularly about intersection 104 so as to provide right angles between adjacent sections. The trace 94 is depicted in the initial plated condition prior to reflow anc comprises an underlying copper layer immediately adjacent substrate 92 and an outer solder electroplate of uniform thickness overlying each section. Thereafter, trace 94 is heated, for example, by immersion in an oil bath, to reflow the solder plate, whereupon the solder is drawn by capillary forces from section 96, 98, 100, and 102 to coalesce at intersection 104 to form a solder bump. The embodiment in FIG. 6 is particularly advantageous

for providing the preferred right angle arrangement between adjacent sections while increasing the volume of solder adjacent the intersection 104.

In the aforedescribed embodiments, the surprising formation of the solder bump is found to occur at an intersection between a first and a second linear section of a circuit trace. The method is particularly suitable for use with sections having widths less than 500 microns, such as is commonly employed in designing circuit traces. The preferred section widths is between about 50 and 150 microns. In these embodiment, sections having equal widths were utilized in forming the bumps. However, sections having different widths may be employed, for example, as necessary to accommodate other design considerations for the electrical circuit. It is believed that optimum conditions for bump formation during reflow are provided by sections arranged so that the angle therebetween is a right angle. However, conditions for forming a suitable bump exist where the angle between the sections is between about 45 degrees and 135 degrees.

In another embodiment of the invention, referring to FIGS. 8-10, the method of this invention is employed to form a printed circuit board 110 having a plurality of solder-bumped terminals for mounting an integrated circuit die component by solder bump interconnections. Printed circuit board 110 comprises a dielectric substrate 112 similar to board 10 in FIGS.1-3. Board 110 further includes a plurality of terminal sections 116 affixed to a planar surface of substrate 112 and surrounded by an adjacent bare region 114. In accordance with this embodiment, each terminal section 116 comprises an enlarged circular terminal pad 118 connected to a linear runner section 120. Runner section 120 extends radially from the circular pad 118 and has a generally uniform width w of

preferably about 100 microns. In the preferred embodiment, terminal pad 118 has a diameter W of about 150 microns.

Referring to FIG. 8, in accordance with the method of this invention, each terminal section 116 is initially fabricated comprising two coextensive metal layers 122 and 124. Layer 122 lies immediately adjacent substrate 112 and is preferably formed of metallic copper having high electrical conductivity conducive to conducting electrical signals. Copper layer 122 is coated by thin layer 124 preferably composed of electroplated tin-lead solder alloy. Printed circuit board 110 is manufactured by masking a copper plate to define the trace, removing the mask to expose the surrounding copper, and etching the exposed copper, whereupon the solder plate serves as a mask in defining the trace, utilizing the process as described for FIG. 1-3.

As initially formed, the printed circuit board comprises a uniform, thin solder plate overlying the trace and is heated to reflow the solder to form the desired bumps. The board is immersed in hot polyoxyalkylene glycol bath at 250 °C for 15 seconds. It was found that during immersion the solder alloy melted and reflowed to draw solder from the linear runner section 120 and accumulate the solder on terminal pad 118, thereby forming a bump 124 shown in FIG. 9. Following reflow, a residual solder film 126 remains on runner 120, but having a thickness substantially reduced compared to the initial film.

FIG. 10 is an electron photomicrograph of a solder bump on a terminal formed in accordance with this embodiment. The height of the bump relative to the copper trace was about 60 microns. Thus, the bump was deemed to be particularly well

suited for use in forming solder bump interconnections to attach an electrical component to the printed circuit board.

Therefore, this embodiment also provides a solder reflow method for producing a solder bump on a terminal pad of a copper trace which requires but a single photoresist mask to define the trace including the terminal pad, which permits the solder to be deposited by electroplating and subsequently used as a mask during etching of the trace, which avoids use of a solder stop by creating conditions that coalesce the solder onto the pad from the adjacent section, and which reduces the plating time by depositing a relatively thin plate and reflowing to accumulate the desired mass for the bump. While not limited to any particular theory, the surprising formation of the bump during reflow is attributed to the particular configuration of the terminal that features an enlarged pad connected to a relatively narrow runner and is effective to cause the molten solder during reflow to be drawn by capillary forces onto the pad from the adjacent runner. In designing the terminal, it is desired to optimize the ratio of the runner width to the pad width to minimize the required thickness of the solder plate while coalescing sufficient solder during reflow to produce the desired bump size. As used herein, the runner width refers to the width of the runner section immediately adjacent the enlarged pad, whereas the pad width refers to the maximum dimension of the pad measured parallel to the runner width. This method is believed to be particularly suitable for use with runners having widths less than about 500 microns, such as is commonly employed in designing circuit traces. The preferred runner width is between about 50 and 150 microns. A pad width, that is, the diameter for the described circular pad, of at least 1.2 times the adjacent runner width is effective in drawing sufficient solder to form a

suitable bump. Preferably, the pad width is between about 1.2 and 2.0 times the runner width.

Referring to FIG. 11, in still another embodiment, a printed circuit board 140 includes a square pad 146 that is in suitable fashion to provide an enlarged area for coalescence of the solder alloy to form a bump. Board 140 including an epoxy-glass substrate 142 and a terminal section 144 that include pad 146 and an adjacent runner 148 that extends from a corner of the square pad. To better illustrate the terminal pad shape, the terminal section is depicted with the solder plate, but prior to reflow to form the bump and thus includes a copper trace and a thin, uniform solder layer similar to the terminal shown in FIG. 8. During reflow, solder is drawn from the runner section onto the terminal pad to produce a generally semispherical bump.

In still a further embodiment, FIG. 12 shows a printed circuit board 160 comprising an epoxy-glass substrate 162 and having a terminal 164 also suitably configured for the practice of this invention. Terminal 164 comprises a generally rectangular pad 166 and an adjacent runner section 168 that extends from a side of pad 166. The terminal is depicted in the condition following elecrodeposition and prior to reflow, similar to the terminal depicted in FIG. 8, to better illustrate the pad configuration. During reflow, solder is drawn onto the terminal pad from the adjacent runner to produce the desired rounded bump.

A significant feature of this invention is the formation of the bump during reflow from an initial thin plate of solder alloy on the trace. While copper is most commonly selected for the trace metal because of its relative low cost and advantageous electrical properties including a low resistance

conducive for conducting electrical signals, the terminal may be formed of any suitable metal that provides a solder-wettable surface, including, for example, nickel or gold, either applied directly onto the dielectric substrate or onto a copper or other metal base to provide an intermediate layer between the base and the solder. The solder layer may be formed of any suitable solder alloy. Typical solder alloys are formed predominantly of one or more metals selected from the group consisting of lead, tin and indium and include lead-base alloys containing about 5 weight percent tin and indium-base alloys containing about 30 percent lead. Preferably, the solder is composed of near-eutectic tin-lead alloy containing between about 35 and 45 percent lead. Although the solder is preferably deposited by electroplating, the plate may be formed by sputtering or any process suitable for applying a thin layer of the solder metal onto the trace.

In the described embodiments, reflow of the thin solder plate also left a residual film on the runner. It is desired to deposit a solder thickness adequate to provide sufficient molten alloy to maximize the bump size. Depending upon the intended application, the residual film on the runner may be advantageous, for example, to provide a protective coating. On the other hand, for a specific trace configuration, it may be desirable to minimize the initial solder deposit to reduce or eliminate the residual film. A solder plate having a thickness less than 25 microns provides sufficient metal during ring reflow for bump formation. Preferably, the initial solder plate thickness is between about 10 and 25 microns. For forming solder bump interconnections, it is desired to produce a bump having a height measured relative to the copper trace surface of at least 40 microns, and preferably between about 60 and 80 microns.

While this invention has been described in terms of certain embodiments thereof, it is not intended that it be limited to the above description but rather only to the extent set forth in the claims that follow. The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows.

1. A method for forming a solder-bumped circuit trace on a dielectric substrate, said method comprising

fabricating a circuit trace on the substrate comprising a first linear section and a second linear section disposed to intersection said first section at intersection so as to form an angle between the sections that is between about 45 degrees and 135 degrees, said trace comprising a solder-wettable metal layer adjacent the substrate and an outer plate composed of a solder alloy and having a uniform thickness, and

heating the circuit trace at a temperature effective to melt the solder alloy and to draw the molten solder alloy onto the intersection to form a solder bump.

2. A method for forming a solder-bumped circuit trace on a dielectric substrate, said method comprising

fabricating a circuit trace on the substrate comprising a first linear section and second linear section, said first section having a generally uniform width less than 500 microns, said second section having a generally uniform width less than 500 microns and being disposed to intersect said fist section at an intersection so as to form an angle between the sections that is between about 45 degrees and 135 degrees, said trace comprising a copper layer adjacent the substrate and an outer plate composed of a tin-lead solder alloy and having a uniform thickness less than about 25 microns, and

heating the circuit trace at a temperature effective to melt the solder alloy and to draw the molten solder alloy onto the intersection to form a solder bump.

3. The method in accordance with claim 2 wherein the first section width is between about 50 and 150 microns.

4. The method in accordance with claim 2 wherein the second section width is between about 50 and 150 microns.

5. The method in accordance with claim 2 wherein the solder plate is an electrodeposited plate composed of an alloy comprising between about 35 and 45 weight percent lead and the balance substantially tin.

6. The method in accordance with claim 2 wherein the solder plate has a thickness between about 10 and 25 microns.

7. The method in accordance with claim 2 wherein the solder bump has a height greater than 40 microns.

8. A method for forming a solder bumped terminal on a planar dielectric substrate comprising

fabricating a terminal on the substrate, said terminal comprising a terminal pad adapted for receiving a solder bump and a linear runner section connected to the pad, said runner section having a predetermined width adjacent the pad, said terminal pad having a width parallel to the section width that is greater than the section width, said terminal comprising a solder-wettable metal layer adjacent the substrate and an outer plate composed of a solder alloy and having a uniform thickness, and

heating the terminal at a temperature effective to melt the solder alloy and to draw the molten solder alloy onto the terminal pad from the adjacent runner section to form a solder bump.

9. A method for forming an electrical circuit trace having a solder-bumped terminal pad on a planar dielectric substrate, said method comprising

fabricating a trace on the substrate, said trace including a dual-plate terminal portion comprising a terminal pad adapted for receiving a solder bump and a linear runner section extending from the pad, said runner section having a predetermined width less than 500 microns, said terminal pad having a width parallel to the runner section width that is at least 1.2 times greater than the runner section width, said terminal portion comprising a copper plate affixed to the substrate and an outer layer composed of tin-lead solder alloy, said copper layer having a uniform thickness, said solder layer having a uniform thickness less than 25 microns, and

heating the terminal at a temperature effective to reflow the solder alloy, whereupon molten solder alloy is drawn onto the terminal pad from the adjacent trace section to form a solder bump having a height of at least 40 microns.

10. The method in accordance with claim 9 wherein the runner section width is between about 50 and 150 microns.

11. The method in accordance with claim 9 wherein the pad width is between about 1.2 and 2.0 times the runner section width.

12. The method in accordance with claim 9 wherein the terminal pad is a circular pad and the runner section extends radially from the pad.

13. The method in accordance with claim 9 wherein the terminal pad is a square pad and the runner section extends from a corner of the pad.

14. The method in accordance with claim 9 wherein the terminal pad is a rectangular pad and the runner section extends from a side of the pad.

15. The method in accordance with claim 9 wherein the solder plate is an electrodeposited plate composed of an alloy comprising between about 35 and 45 weight percent lead and the balance substantially tin.

16. The method in accordance with claim 9 wherein the solder plate has a thickness between about 10 and 25 microns and the solder bump height is between about 60 and 80 microns.

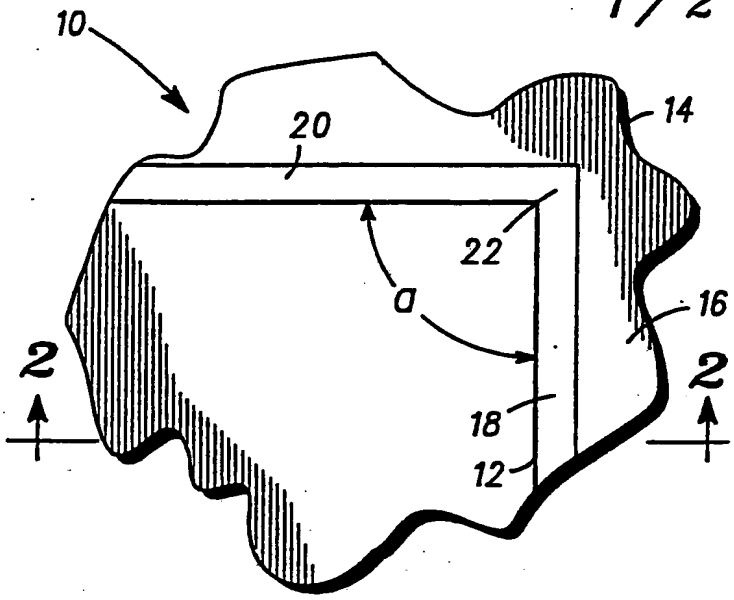

FIG. 1

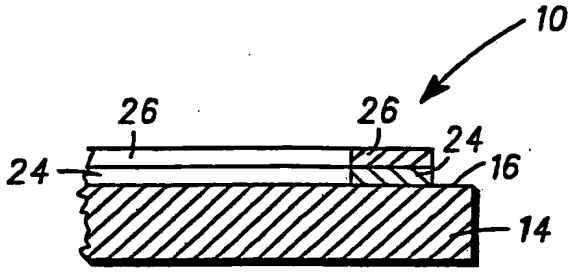

FIG. 2

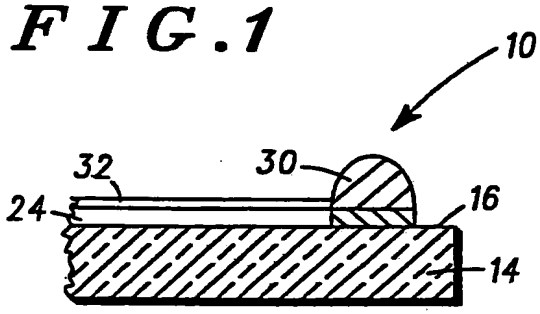

FIG. 3

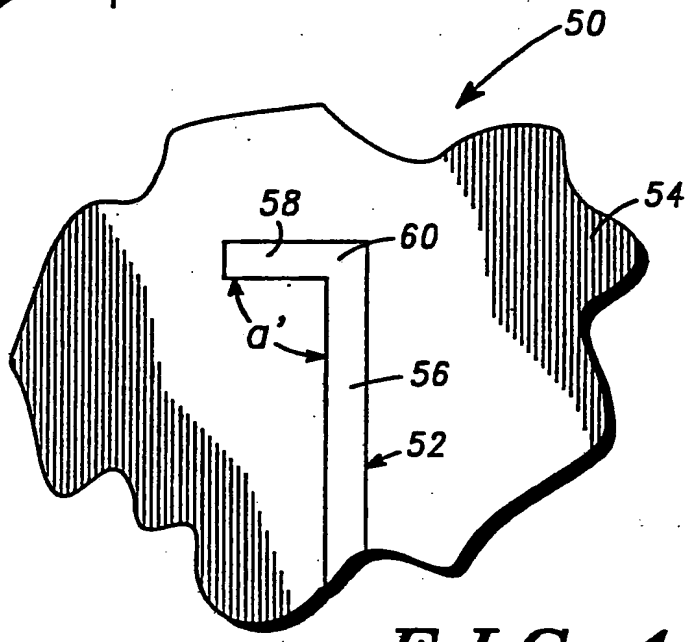

FIG. 4

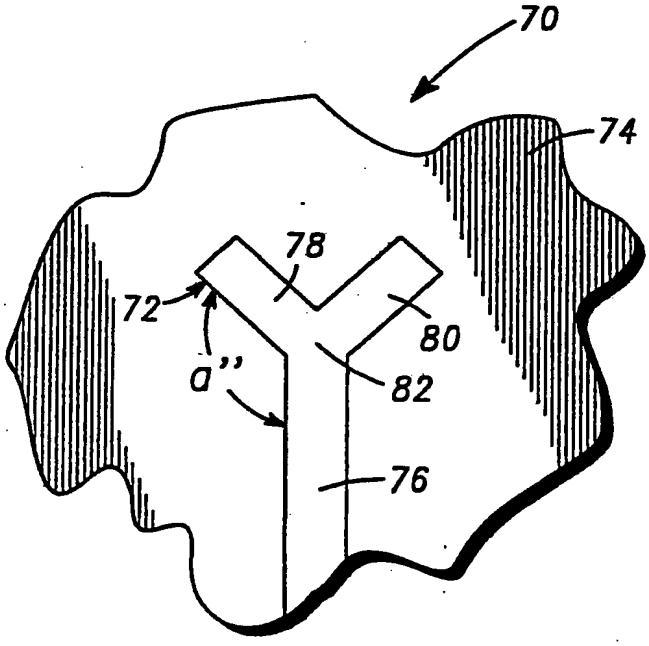

FIG. 5

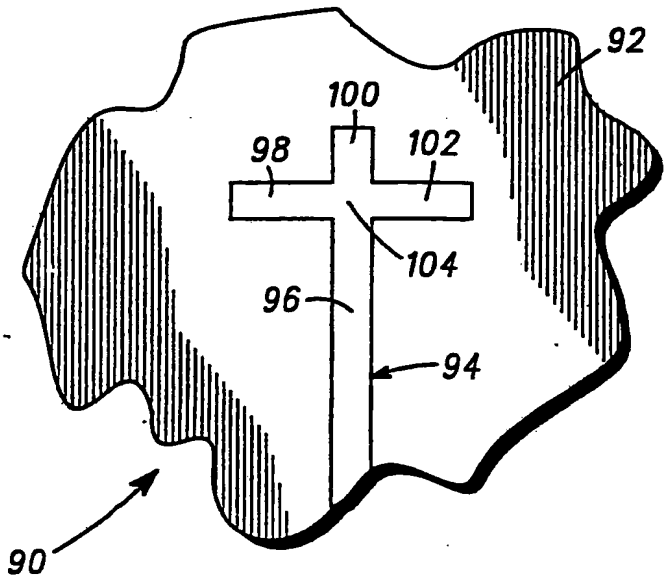

FIG. 6

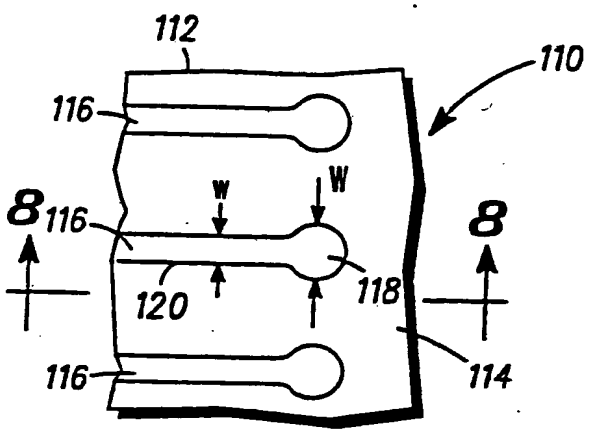

FIG.7

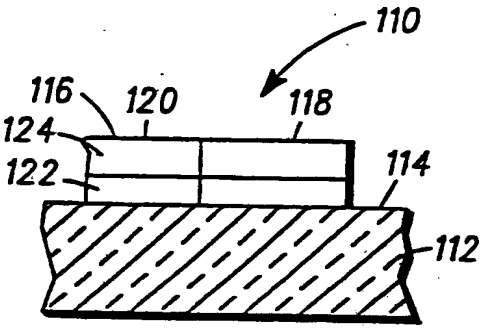

FIG.8

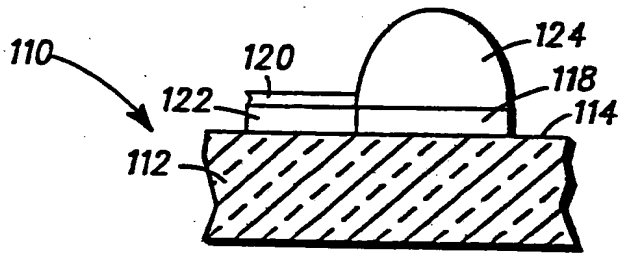

FIG.9

FIG.10

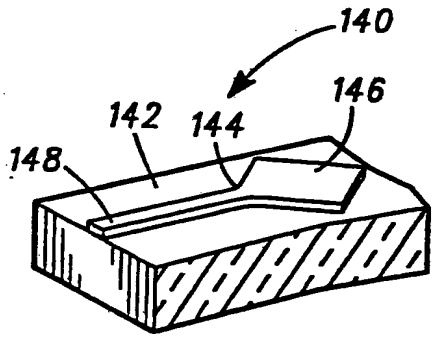

FIG.11

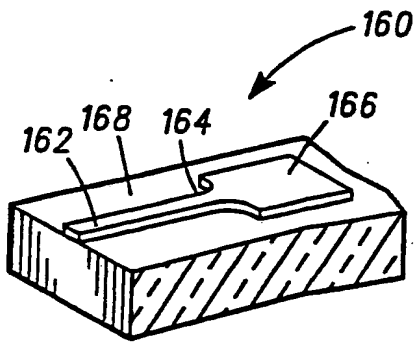

FIG.12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/06456

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :B23K 31/02; B44C 1/22; H05K 3/00
US CL :029/843,846; 156/901; 228/180.1
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 029/860; 156/634,656,902; 228/180.2

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A, 3,429,040 (MILLER), 25 FEBRUARY 1969, See col. 2 lines 15-37.	1-16
A	US,A, 4,978,423 (DURNWITTH ET AL), 18 DECEMBER 1990, See col. 1, lines 30-39.	1-16

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

25 SEPTEMBER 1992

Date of mailing of the international search report

09 NOV 1992

Name and mailing address of the ISA/
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

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